ABSTRACT OF THE DISCLOSURE

A semiconductor device with a CMOS transistor structure in which a gate electrode and a wire connecting an N^+-type active region and a P^+-type active region overlap each other in plan view, to reduce a footprint of the CMOS transistor structure, is provided. An N^+-type active region (1) of an n-channel MOS transistor and a P^+-type active region (2) of a p-channel MOS transistor are formed in a surface portion of a semiconductor substrate by ion implantation or the like. Gate electrodes (3) are formed on the N^+-type active region (1) and the P^+-type active region (2). Insulating films (4, 5) of silicon nitride are formed on the gate electrodes (3). An interlayer insulating film (6) of silicon oxide is formed over the gate electrodes (3) covered with the insulating films (4, 5), by CVD or the like. Openings (7) for accommodating wires connecting the N^+-type active region (1) and the P^+-type active region (2) are formed in the interlayer insulating film (6). A metal film such as an aluminum film is buried in the openings (7), to form buried wires (8).